C. Amendments to the Drawings.

FIG. 6D has been amended to change label "614-d" to "614-c".

5

D. Remarks

Rejection of Claims 1-3 and 5 Under 35 U.S.C. §102(b) based on U.S. Patent No. 5,780,910 (*Hashimoto et al.*).

Amended claim 1 is directed to a memory cell that includes a first node for storing a first potential, a second node for storing a second potential, transistor gates formed from a gate layer, and a capacitor having plates coupled between the first node and second node. A portion of one plate of the capacitor includes a first interconnect wiring formed over the gate layer that includes a plurality of conductive layers and that electrically interconnects circuit devices of the memory cell.

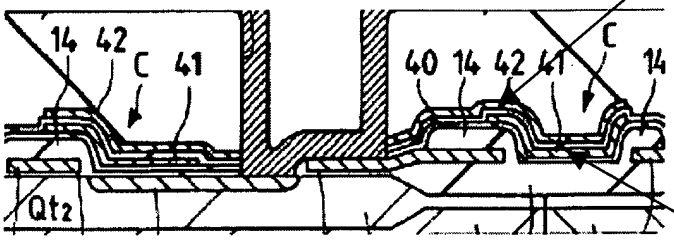
As is well established, anticipation requires the presence of a single prior art reference disclosure of each and every element of the claimed invention, arranged as in the claim. There must be no difference between the claimed invention and the reference disclosure, as viewed by a person of ordinary skill in the field of the invention.[1]

As emphasized above, claim 1 recites "a first interconnect wiring". This first interconnect wiring includes "a plurality of conductive layers" and "electrically interconnects circuit devices of the memory cell". Applicants do not believe that the cited reference shows or suggests such claim limitations.

Hashimoto et al. shows a static random access memory (SRAM) with a capacitor element having a stacked structure. The various capacitors shown in *Hashimoto et al.* are formed by a lower electrode separated from an upper electrode by a capacitor insulating film. However, in the various examples of *Hashimoto et al.* the lower and upper electrodes include a single polycrystalline silicon (polysilicon) film, as opposed to "a plurality of conductive layers".

In addition, the capacitor electrode structures of *Hashimoto et al.* do not "electrically interconnect" circuit devices of the memory cell, as such electrodes are electrically connected only to a single node, and not between memory cell devices. These differences are illustrated in the portion of FIG. 36 from *Hashimoto et al.* shown below. It is noted that the remaining capacitor examples from the cited reference show this same single layer capacitor electrode construction.

[1] Scripps Clinic & Research Found. v. Genetech Inc., 18 USPQ 2d 1001, 1010 (Fed. Cir. 1991).



Upper capacitor electrode 42 is formed from a single film:

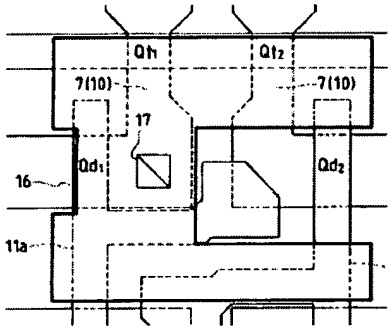
"[A]n n-type polycrystalline silicon film... is... patterned to form the upper electrode 42 of the capacitor element C.

Lower capacitor electrode 41 is also formed from a single film:

"***[T]he*** n-type polycrystalline silicon film... is patterned to form the lower electrode 41 of the capacitor element C." (*Hashimoto et al.*, Col. 19, Lines 23-25).

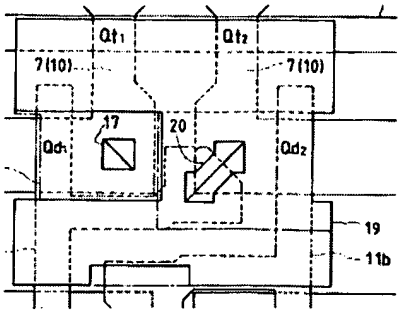
Accordingly, because the reference teaches capacitor electrode formed from single films, Applicants' do not believe that the reference shows or suggests "a plurality of conductive layers" as recited in claim 1.

In addition, the capacitor electrode structures from *Hashimoto et al.* do not "electrically interconnect" any circuit devices of a memory cell. Both capacitor electrodes of *Hashimoto et al.* are electrically connected to a single node, and provide no interconnection between circuit devices. This is best illustrated by FIGS. 2(c) and 2(d), which show each capacitor electrode has only a single connection to one device terminal.



Lower capacitor electrode 16 has a single electrical connection, thus cannot interconnect two devices.

"The lower electrode 16 is connected through contact hole 17 to the drain region... of driver MISFET Qd1..." (*Hashimoto et al.*, Col. 12, Line 66 to Col. 13, Line 2).



Upper capacitor electrode 19 also has a single electrical connection, thus cannot interconnect two devices.

"The lower electrode 19 is connected through contact hole 20 to the gate electrode 11a..." (*Hashimoto et al.*, Col. 13, Lines 7-9).

Accordingly, because the reference teaches capacitor electrodes having but single electrical connections, the reference is not believed to show or be suggestive of Applicants' "one plate of the capacitor" that includes a first interconnect wiring "that electrically interconnects circuit devices".

For all of these reasons, the cited reference is not believed to show or suggest every element of Applicants claimed invention as arranged in claim 1, and this ground for rejection is traversed.

Amended claim 5, which depends from claim 1, recites that the first interconnect wiring includes a plurality of separate portions, each portion including a bottom conductive layer, a dielectric layer formed over the bottom conductive layer, and a top conductive layer formed over the dielectric layer. The top conductive layer forms at least a portion of the first plate of the capacitor.

As understood from the above comments, *Hashimoto et al.* shows a capacitor structure that includes a top electrode, a bottom electrode, and a capacitor dielectric. However, this capacitor structure is a unitary structure. Consequently, the cited reference is not believed to show or suggest "a plurality of separate portions", as recited in amended claim 5.

For these reasons, claim 5 is believed to be separately patentable over the cited reference.

Rejection of Claim 6 Under 35 U.S.C. §103(a) based on U.S. Patent No. 5,780,910 (*Hashimoto et al.*).

Claim 6, which depends indirectly from claim 1 via claim 5, recites that the memory cell further includes a second conductive interconnect wiring formed over the first conductive

interconnect wiring that forms at least a portion of a second plate of the capacitor.

As is well known, to establish a prima facie case of obviousness, a rejection must meet three basic criteria. First, there must be some suggestion or motivation to modify a reference or combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference(s) must teach or suggest all claim limitations.[2]

Further, obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found in either the references themselves or in the knowledge generally available to one of ordinary skill in the art.[3]

To arrive at Applicants' claim 6 invention, the rejection relies on the following reasoning:

> It would have been obvious... to [modify] Hashimoto et al. accordingly by utilizing a second wiring layer in order to provide conductivity between components of the semiconductor memory device. (See the Office Action, dated 8/15/06, Page 5, Section 5, Last Paragraph).

The above motivation does not appear to be from *Hashimoto et al.* and no official notice has been taken. Accordingly, Applicants do not believe it is sufficient to establish a prima facie case of obvious.

It is Applicants' invention which advantageously utilizes an interconnect wiring to form first and second plates of a capacitor. Thus, the only apparent rationale for the suggested modification would appear to arise from the teachings of present application. This would constitute impermissible hindsight as a source of motivation.

Accordingly, because the proposed suggestion/motivation appears insufficient to establish a prima facie case for claim 6, this claim is believed to be separately patentable over the cited reference.

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[2] MPEP §2143.

[3] See In re Fine, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988); see In re Jones, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992).

New Claims 21 to 23

New claim 21, which depends from claim 1, recites that the gate layer is not in physical contact with a drain of any transistor of the memory cell. The Specification provides clear support for this claim, and thus presents no new matter.[4]

Hashimoto et al. shows an arrangement in which gate electrodes are in physical contact with drains of transistors. This is best shown in FIG. 2(b) of the cited reference, where gate electrode 11(a) is in contact with a drain region of transistor Qd_2, and gate electrode 11(b) is in contact with a drain region of transistor Qp_1.

New claim 22, which depends from claim 1, recites that a first portion of the first interconnect wiring is in physical contact with the drains of a first and second transistor of the memory cell. In addition, a second portion of the first interconnect wiring, different from the first portion, is in physical contact with the drains of third and fourth transistor of the memory cell. The Specification provides clear support for this claim, and thus presents no new matter.[5]

Hashimoto et al. teaches a single capacitor element. Accordingly, such a single element cannot show first and second portions of a first interconnect wiring. *Hashimoto et al.* also shows local wiring lines L_1 and L_2. These local wirings, however, form no portion of the capacitor element.

New independent claim 23 recites a memory cell that includes a first data storage node, a second data storage node, and a capacitor. The capacitor comprises a first plate coupled to the first data storage node, a second plate coupled to the second data storage node, and a third plate separated from the first and second plates by a capacitor dielectric. The first and second plates comprise portions of an interconnect layer that electrically connects terminals of transistors of the memory cell to one another. The Specification provides clear support for this claim, and thus presents no new matter.[6]

Independent claim 23 recites three capacitor plates. As understood from the above discussion of *Hashimoto et al.*, the cited reference shows a capacitor element with only two capacitor electrodes. Thus, the cited art is not believed to show or suggest Applicants three plate structure.

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[4] See Applicants' FIG. 7A, which shows gate layer portions 710/712 not in physical contact with any transistor drain.

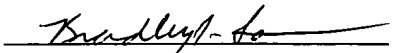
[5] See Applicants' FIG. 7A, which shows wiring portions 714/716, each in physical contact with two different transistor drains.

[6] See Applicants' FIG. 4E, which shows capacitors C1/C2 formed with three capacitor plates.

Claims 1 and 5-6 have been amended. New claims 21-23 have been added. Claim 6 has been amended to correct an error in claim dependency, and not in response to the cited art.

The present claims 1-3, 5-7 and 21-23 are believed to be in allowable form. It is respectfully requested that the application be forwarded for allowance and issue.

Respectfully Submitted,



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